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**DATE:** May 6, 2003

TECHNOLOGY CENTER 2800

**PTO IDENTIFIER:** Application Number 09/387,857-Conf. #3099  
Patent Number**Inventor:** Fumitaka Sugaya**MESSAGE TO:** C. Novacek**FAX NUMBER:** (703) 872-9318**FROM:** CONNOLLY BOVE LODGE & HUTZ LLP

George R. Pettit

**PHONE:** (202) 331-7111**Attorney Dkt. #:** 21776-00039-US**PAGES (Including Cover Sheet):** 11**CONTENTS:**

In response to the Office Action mailed February 6, 2003, Applicant wish to file the attached Amendment.

If your receipt of this transmission is in error, please notify this firm immediately by collect call to (202) 331-7111 and send the original transmission to us by return mail at the address below.

**CONNOLLY BOVE LODGE & HUTZ LLP**

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PTO/SB/97 (12-97)

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Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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on May 6, 2003  
Date

  
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Deborah A. Harrell  
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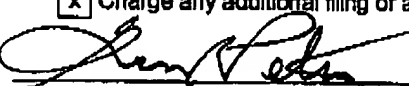
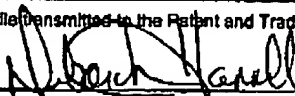
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must identify each submitted paper.

Amendment in Response to Non-Final Office Action;  
Amendment; and  
Amendment Transmittal.

<b>AMENDMENT TRANSMITTAL LETTER</b>				Docket No. 21776-00039-US	
Application No. 09/387,857-Conf. #3099	Filing Date September 1, 1999	Examiner C. Novacek	Art Unit 2822		
Applicant(s): Fumitaka Sugaya					
Invention: A SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME					
<b>TO THE COMMISSIONER FOR PATENTS</b>					
Transmitted herewith is an amendment in the above-identified application. The fee has been calculated and is transmitted as shown below.					
<b>CLAIMS AS AMENDED</b>					
	Claims Remaining After Amendment	Highest Number Previously Paid	Number Extra Claims Present	Rate	
Total Claims	18	- 20 =	0	x	0.00
Independent Claims	5	- 5 =	0	x	0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					
Other fee (please specify):					
<b>TOTAL ADDITIONAL FEE FOR THIS AMENDMENT:</b>					0.00
<input checked="" type="checkbox"/> Large Entity <span style="margin-left: 200px;"><input type="checkbox"/> Small Entity</span>					
<input checked="" type="checkbox"/> No additional fee is required for this amendment. <span style="float: right;">FAX RECEIVED MAY 06 2003 TECHNOLOGY CENTER 2800</span>					
<input type="checkbox"/> Please charge Deposit Account No. _____ in the amount of \$ _____. A duplicate copy of this sheet is enclosed.					
<input type="checkbox"/> A check in the amount of \$ _____ to cover the filing fee is enclosed.					
<input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.					
<input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge and credit Deposit Account No. <u>22-0185</u> as described below. A duplicate copy of this sheet is enclosed.					
<input checked="" type="checkbox"/> Credit any overpayment.					
<input checked="" type="checkbox"/> Charge any additional filing or application processing fees required under 37 CFR 1.16 and 1.17.					
 George R. Pettit Attorney Reg. No.: 27,389 CONNOLLY BOVE LODGE & HUTZ LLP 1990 M Street, N.W., Suite 800 Washington, DC 20036-3425 (202) 331-7111				Dated: <u>May 6, 2003</u>	
I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office, facsimile no. (703) 872-9318, on the date shown below. Dated: <u>May 6, 2003</u>					
Signature:  (Deborah A. Harrell)					

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Dated: May 8, 2003

Signature: 

(Deborah A. Harrell)

# 17/E  
Diking  
5-7-03Docket No.: 21776-00039-US  
(PATENT)

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Fumitaka Sugaya

Application No.: 09/387,857

Group Art Unit: 2822

Filed: September 1, 1999

Examiner: C. Novacek

For: A SEMICONDUCTOR DEVICE AND A  
METHOD OF MANUFACTURING THE SAMEAMENDMENTCommissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

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Dear Sir:

In response to the Office Action dated February 6, 2003 (Paper No. 16), please amend the above-identified U.S. patent application as follows:

IN THE CLAIMS:

Kindly amend the claims as follows:

- E' 32. (Amended) A method of fabricating a semiconductor device, comprising:
- the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;
  - the second step of forming a gate insulating film and a gate electrode in said element active region;
  - the third step of doping an impurity into said active region of said substrate to form a pair of impurity diffusion layers in surface regions of said semiconductor substrate on two sides of said gate electrode;